Career Objective: To become a key resource for an institution, where I can explore my full potential, add to my learning curve, as well as contribute effectively and efficiently to achieve institution goals. To make the best use of my technical expertise in logic development & data analysis in academic and research based career. Looking for a career with the teaching and research having a global vision, which encourages creativity. .	

1.	Name in Full	**PUJA GHOSH**

2. Educational Qualifications

Sl. No.	Degree Obtained	Discipline	Name of the University/Institute	Year of Passing	% of Marks/ CGPA	Class/ Division
(i)	Ph.D.	VLSI	NIT Silchar	2020	7.6	1st
(ii)	M. Tech	ECE	NIT Meghalaya	2017	9.6	1st
(iii)	B. Tech.	ETC	KIIT University	2015	8.49	1st
(iv)	XII Class	Physics, Chemistry, Maths	Chinmaya Vidyalaya	2011	87.2 %	1st
(v)	X Class	Maths, Science, English	Bal Mandir Senior Secondary School	2009	90.8 %	1st
(vi)	Other if any					

3. Ph.D. Degree Details

(i) Ph.D. Thesis Title	Bandgap Engineered Selective Buried Oxide Tunnel FETs: Simulation, Modeling and Applications
(ii) Research area of Ph.D. Thesis work	Low Power Semiconductor Device (VLSI)
(iii) Name(s) of Supervisor(s) & Address	Dr. Brinda Bhowmick, Associate Professor, ECE, NIT Silchar

4. M.TechDegree Details

(i) M.Tech Dissertation Title	Design and Implementation of TernaryContent Addressable Memory (TCAM) based Hierarchical Motion Estimation for Video Processing
(ii) Area of M.Tech.Dissertation work	VLSI Design
(iii) Name(s) of Supervisor(s) & Address	Dr. P. Rangababu, Assistant Professor, NIT Meghalaya

5. Number of Publications:

Nature		Published (SCI)	In-Press (SCI)
(i) Refereed Journals	National (SCI)	1	
	International (SCI)	12	
	National (Scopus)		
	International (Scopus)		
(ii) Conference Proceedings	SCI	2	
	Scopus		
	Web of Sciences		

6. Reviewer of Journals

Name of the Journal	Name of the Publisher	National /International
Microelectronics Journal	Elsevier	International
International Journal of Electronics	Taylor & Francis	International
International Journal of RF and Microwave Computer-Aided Engineering	Wiley	International

7. Number of Awards/Prizes/Medals/Achievements:

Awarded (Title)	Gold Medalist (M. Tech)
Proposed, if any	Qualified in Graduate Aptitude Test in Engineering (GATE)
Achievement	Speaker of Workshop on Recent Trends in Microelectronic Devices, VLSI Circuits & Their Applications, Organized by Microelectronics Research Group (MERG), K. L. University

8. Technical Skill:

Tools	Synopsys TCAD, Xilinx ISE, Cadence

9. Extra-Curricular Activities

Student Volunteer at International Conference on innovations in Electronics, Signal Processing and Communication (IESC), 2017
Student Volunteer at International Conference on Recent Trends on Electronics and Computer Science (ICRTECS), 2019.

10. Number of Short-Term Courses/Workshop/ Symposiums/Seminars Attended:

Type of the Course/Workshop/etc.	Name of the Course/Workshop/etc.	Sponsoring Agency	Period of Course	Coordinator/ Co-Coordinator
Course	Algorithms and Architectures for High Efficiency Video Coding	MHRD	5th-9th September, 2016	TEQIP
Workshop	Modeling of Novel Nanoelectronic Devices and Circuits for ULSI Technology	DST-SERB and TEQIP-III	26-30 April, 2019	IEEE, EDS
Workshop	Nanofabrication Technologies	INUP	28-29, January, 2019	Meity Government of India

11. Membership/Fellowship in Professional Bodies if any

Name of the Professional Body	Membership status(Life/ Annual)
IEEE Electron Devices Society	Annual

12. Name of two referees with complete contact details including address, Tel. Nos., Fax Nos., Email address

(i) Dr. Brinda Bhowmick, Associate Professor, ECE, NIT Silchar, 9954806903, brindabhowmick@gmail.com

(ii) Dr. P. Rangababu, HOD &Assistant Professor, NIT Meghalaya, 8837225547, p.rangababu@gmail.com

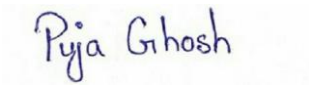
13. List of Research Journals (SCI/Scopus) :

(i)	P. Ghosh and B. Bhowmick, "Investigation of Electrical Characteristics in a Ferroelectric L-patterned Gate Dual Tunnel Diode TFET," *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, pp. 1-6, 2020.
(ii)	P. Ghosh and B. Bhowmick, "Analysis of kink reduction and reliability issues in low-voltage DTD-based SOI TFET," *Micro & Nano Letters*, vol. 15, pp. 130-135, 2020.
(iii)	P. Ghosh and B. Bhowmick, "Effect of temperature in selective buried oxide TFET in the presence of trap and its RF analysis," *International Journal of RF and Microwave Computer-Aided Engineering*, vol. 30, pp. 1-9, 2020.
(iv)	P. Ghosh, A. Roy, and B. Bhowmick, "The impact of donor/acceptor types of interface traps on selective buried oxide TFET characteristics," *Applied Physics A*, vol. 126, pp. 1-7, 2020.
(v)	P. Ghosh and B. Bhowmick, "Deep insight into material-dependent DC performance of Fe DS-SBTFET and its noise analysis in the presence of interface traps,"*AEU- International Journal of Electronics and Communications*, vol. 117, pp. 153124(1-7), 2020.
(vi)	P. Ghosh and B. Bhowmick,"Optimization of Ferroelectric SELBOX TFET and Ferroelectric SOI TFET,"*ECS Journal of Solid State Science and Technology*, vol. 9,pp.023001, 2020.
(vii)	P. Ghosh, R. Goswami, and B. Bhowmick, "Optimization of ferroelectric tunnel junction TFET in presence of temperature and its RF analysis", *Microelectronics Journal*, vol. 92, pp.104618 (1-5), 2019.
(viii)	P. Ghosh and B. Bhowmick, "Reduction of the kink effect in a SELBOX tunnel FET and its RF/analog performance," *Journal of Computational Electronics*, vol. 18, pp. 1182-1191, 2019.
(ix)	P. Ghosh and B. Bhowmick, "Effect of Temperature on Reliability Issues of Ferroelectric Dopant Segregated Schottky Barrier Tunnel Field Effect Transistor (Fe DS-SBTFET)," *Silicon*, vol. 12, pp. 1137-1144, 2019.
(x)	P. Ghosh and B. Bhowmick, "Optimisation of electrical parameters in Fe DSSBTFET and its application as a digital inverter," *International Journal of Electronics*, vol. 106, pp. 1617-1631, 2019.
(xi)	P. Ghosh and B. Bhowmick, "Noise behaviour of δp^+ $Si_{1-x}Ge_x$ layer SELBOX TFET," *Indian Journal of Physics*,

		vol. 94, pp. 493-500, 2019.
	(xii)	P. Ghosh and B. Bhowmick, "Low-frequency noise analysis of heterojunction SELBOX TFET," *Applied Physics A*, vol. 124, pp. 1-9, 2018.
	(xiii)	P. Ghosh and B. Bhowmick, "An Analytical Model of surface potential and capacitance in Heterojunction SELBOX TFET," *International Journal of Numerical Modelling: Electronic Networks, Devices and Fields*, 2021.
14.	List of Conferences:	
	(i)	P. Ghosh, and P. Rangababu, "Design and Implementation of Ternary Content Addressable Memory (TCAM) Based Hierarchical Motion Estimation for Video Processing," In *International Symposium on VLSI Design and Test*, pp. 557-569, Springer, 2017.
	(ii)	P. Ghosh, B. Bhowmick, "The Impact of Interface Traps (acceptor/donor) on Fe DS-SBTFET Characteristics," In *TENCON 2019-2019 IEEE Region 10 Conference (TENCON)*, pp. 73-77, IEEE, 2019.

DECLARATION

I hereby, solemnly declare that the information furnished in this application are true and correct to the best of my knowledge and belief. If at any time I am found to have concealed/ suppressed any material/ information or given any false details, my appointment shall be liable to be summarily terminated without notice of compensation.



Signature of the Applicant