CURRICULUM VITAE

PRIYABRAT GARANAYAK
Assistant Professor Grade – II,
Dept. of Electronics and Communication Engineering,
Indian Institute of Information Technology Ranchi

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Research Interests:

Active and Hybrid Filters, Uninterruptible Power Supply (UPS), Adaptive Signal Processing Applied to Power Systems, Renewable Power Generation, DC Microgrid, and Electric Vehicle Charging Infrastructure.

Prospective Students:

For research, I am now looking for highly motivated students with a background in Power Electronics and Signal Processing. Students that are interested in my research should look through my publications. Please include your CV in the email, outlining your areas of interest and experience.

Teaching Interests:

Semiconductor Devices and Circuits, Analog Electronics, Linear Integrated Circuits, Digital System Design, VLSI Design, HDL and High-Level Synthesis, Embedded System, Signals and Systems, Adaptive Signal Processing, Electric Circuits and Networks, Control System, Power Electronics, Electric Power Quality, and Renewable and Sustainable Energy System.

Education:

PhD in Electrical and Electronics Engineering (2016),
National Institute of Technology Meghalaya, India
Thesis: Power Quality Assessment and its Enhancement in a Distribution Power System Network
Supervisor: Prof. Gayadhar Panda (Professor, NIT Meghalaya)

M. Tech. in VLSI and Embedded System Design (2011),
Centre for Advanced Post Graduate Studies (Formerly, Centre for Microelectronics),
Biju Patnaik University of Technology, Odisha
Thesis: Design and Implementation of Adaptive Noise Canceller
Supervisor: Dr. Tapas Kumar Patra (Associate Professor, CET Bhubaneswar) and
Prof. Jitendra Kumar Das (Professor, KIIT University)

B.Tech. in Electronics and Telecommunication Engineering (2009),
Biju Patnaik University of Technology, Odisha

Research Experiences:

— Project Associate at ***Indian Institute of Technology Delhi***, India, from August 2016 to July 2017 (Post-PhD).

— Junior Research Fellow at ***National Institute of Technology Meghalaya***, India, from September 2013 to January 2014.

Teaching Details:

— Assistant Professor Grade – II Level-10 at ***Indian Institute of Information Technology Ranchi***, Jharkhand, India, from March 2023 to till date (Post-PhD).

— Ad-hoc Faculty at ***Indian Institute of Information Technology Ranchi***, Jharkhand, India, from January 2022 to March 2023 (Post-PhD).

— Assistant Professor (On Contract Basis) at ***Indian Institute of Information Technology Una***, Himachal Pradesh, India, from July 2018 to December 2021 (Post-PhD).

— Assistant Professor (On Contract) at ***Indian Institute of Information Technology Pune***, Maharashtra, India, from July 2017 to June 2018 (Post-PhD).

— Lecturer (Contractual) at ***Indira Gandhi Institute of Technology Sarang***, Odisha, India, from February 2013 to August 2013.

Journals (SCI/SCIE):

— P. Shaw and **P. Garanayak**, "Design and analysis of an improved voltage-lift-based extended quadratic gain boost converter with reduced voltage stress across components", *International Journal of Circuit Theory and Applications*, pp. 1–22, Dec. 2023, https://doi.org/10.1002/cta.3880.

— **P. Garanayak**, R. T. Naayagi, and G. Panda, "A High-Speed Master-Slave ADALINE for Accurate Power System Harmonic and Inter-Harmonic Estimation", *IEEE Access*, vol. 8, pp. 51918–51932, Mar. 2020.

— **P. Garanayak**, G. Panda, and S. Mishra, "Harmonic Elimination Using SW Based HSAPF System and Evaluation of Compensation Effect Employing ADALINE-DFFRLS Algorithm", *EPE Journal: European Power Electronics and Drives (Taylor and Francis)*, vol. 29, no. 2, pp. 64–81, Apr. 2019.

— P. Shaw and **P. Garanayak**, "Analysis, Design and Implementation of Analog Circuitry Based Maximum Power Point Tracking for Photovoltaic Boost DC/DC Converter", *Transactions of the Institute of Measurement and Control (SAGE)*, vol. 41, no. 3, pp. 668–686, Feb. 2019.

— **P. Garanayak** and G. Panda, "An adaptive linear neural network with least mean M-estimate weight updating rule employed for harmonics identification and power quality monitoring", *Transactions of the Institute of Measurement and Control (SAGE)*, vol. 40, no. 6, pp. 1936–1949, Apr. 2018.

— **P. Garanayak** and G. Panda, “Fast and accurate measurement of harmonic parameters employing hybrid adaptive linear neural network and filtered-x least mean square algorithm”, *IET Generation, Transmission & Distribution*, vol. 10, no. 2, pp. 421–436, Feb. 2016.

— **P. Garanayak**, G. Panda, and P. K. Ray, “Harmonic estimation using RLS algorithm and elimination with improved current control technique based SAPF in a distribution network”, *International Journal of Electrical Power & Energy Systems (Elsevier)*, vol. 73, pp. 209–217, Dec. 2015.

— **P. Garanayak** and G. Panda, “Harmonic elimination and reactive power compensation by novel control algorithm based active power filter”, *Journal of Power Electronics (Springer)*, vol. 15, no. 6, pp. 1619–1627, Nov. 2015.

Conferences:

— **P. Garanayak**, K. P. Panda, R. T. Naayagi, and G. Panda, “An Ultra-Fast Master-Slave ADALINE for Hybrid Active Power Filter including Photovoltaic System”, *3rd International Conference on Energy, Power and Environment (ICEPE 2020)*, pp. 1–6, Mar. 2021.

— **P. Garanayak**, G. Panda and P. K. Ray, “Power System Harmonic Parameters Estimation using ADALINE-VLLMS Algorithm”, *1st International Conference on Energy, Power and Environment (ICEPE 2015)*, pp. 1–6, Jun. 2015.

Researcher Profile:

— Researcher ID: https://www.webofscience.com/wos/author/record/791245

— Scopus ID: https://www.scopus.com/authid/detail.uri?authorId=56658730200

— ORCID ID: https://orcid.org/0000-0003-2993-5494

— Google Scholar: https://scholar.google.co.in/citations?user=BKysQGUAAAAJ&hl=en

— ResearchGate: https://www.researchgate.net/profile/Priyabrat-Garanayak

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Technical Tools:

— Software Development Tool: Matlab/Simulink, Vivado Design Suite, OrCAD PSpice.

— Hardware Tool: Xilinx Artix-7 FPGA, Arduino UNO, Spartan-3A DSP.

Achievements and Awards:

— Awarded SERB National Post-Doctoral Fellowship (NPDF) for the project entitled "Proposal of a New Generation Power Converter for Harmonic Elimination, Reactive Power Compensation and Load Balancing in Medium Voltage Applications". Duration: 2 Years, Approved Fund: 19,20,000.00, File Number: PDF/2017/375/ES.

— Awarded MHRD Fellowship during PhD at NIT Meghalaya.

— Qualified GATE 2010, 2011 in ECE.

Responsible Work at IIIT Ranchi:

- Nodal Officer (April 2023 – Present)
- Faulty Advisor of 2nd Year EC & IOT (May 2023 – Present)
- Program Coordinator, Executive M.Tech. in Autonomous Connected Electric Vehicle (August 2022 – Present)
- Hostel Warden (December 2023 – Present)

Extension Works:

- Reviewer of IEEE Transactions on Industrial Electronics, IEEE Transactions on Industrial Informatics, IEEE Transactions on Circuits and Systems I: Regular Papers, IET Generation, Transmission & Distribution, International Journal of Electrical Power & Energy Systems, Electric Power Components and Systems.
- Session Chair of IEEE ICICCSP – 2022, IEEE ICEPE – 2020.

Collaborations:

- **Prof. Gayadhar Panda**, Professor,
  National Institute of Technology Meghalaya.
- **Dr. Thaiyal Naayagi Ramasamy**, Associate Professor,
  Newcastle University in Singapore.
- **Prof. Sukumar Mishra**, Professor,
  Indian Institute of Technology Delhi, India.
- **Prof. Pravat Kumar Ray**, Professor,
  National Institute of Technology Rourkela.
- **Dr. Priyabrata Shaw**, Senior Engineer
  Energy Systems, Eaton Research Labs (ERL), Pune
- **Mr. Debasish Mishra**, Senior Engineer,
  R & D Hitachi Energy, Chennai

Last update on 11th January 2024

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