Date: 18/03/2026

Syllabus/ Mode of Selection for the Post of Deputy Registrar with reference to the Advt. No: IIITR/RG/2026/Advt./01 Date: 30.01.2026

Group – A

1. **Deputy Registrar:**

In view of the large number of applications received for the post of Deputy Registrar, the Institute has decided to conduct a Screening Test. The selection process shall consist of two stages, namely: **Stage–I: Domain Screening Test**, which will be conducted only for the purpose of shortlisting of the candidates for **Stage–II (Personal Interview).**

Stage–I: Screening Test – The test shall consist of two parts, with no negative marking as detailed below:

➢ **Part–A: MCQ Type Questions (50 Questions carrying 50 marks, 1-hour duration).**
➢ **Part–B: Descriptive Questions and Case Studies (50 marks, 1-hour duration).**

- General Awareness and Current Affairs
- **Aptitude Test -** Quantative Aptitude, Numerical Ability, Data Interpretation, Logical Reasoning & Computer Aptitude.
- **English -** Grammar & Comprehension.
- Constitution of India.
- General Awareness related to IIIT Ranchi as per the data mentioned on the website.
- IIIT (PPP) Act and Statutes of IIIT Ranchi.
- UG, PG and Ph.D. Ordinances of IIIT Ranchi.
- Policies and Regulatory Bodies of Govt. of India on Higher Technical Education.
- RTE Act, RTI Act 2005, Goods and Services Tax (GST), National Education Policy (NEP) 2020, National Pension Scheme (NPS), General Provident Fund (GPF)
- FR and SR rules covering Service Matter, Pay Fixation, TA/DA rules, LTC Rules, Foreign Services, Deputation, Lien, Advances.
- Allowances including Children Education Allowance (CEA), Medical Attendance Rules (CGHS & CSMA)
- CCS (Pension) Rule, CCS (Conduct) Rule, CCS (CCA) Rule, CCS (Leave) Rule.
- Provision of Central Government Accounts (Receipts and Payments) Rules.
- Income Tax Act 1961 along with Financial Act.
- Recruitment and Reservation Rules.
- Budget and Accounting in Autonomous Bodies.

- General Financial Rules (GFR) 2017 and its subsequent amendments, Policies and rules for Procurement of Goods and Services, CPPP and GeM Portal, Delegation of Financial Rules.
- Rajbhasha Adhiniyam

Stage – II: Personal Interview

The Personal Interview shall be conducted by the Selection Committee to examine the suitability of the candidates for the said post, inter alia, on the basis of their academic qualifications, domain expertise, relevant experience, general awareness, communication skills, and overall personality.

The final merit list shall be prepared solely on the basis of the candidate's performance in the Personal Interview (Stage–II).

Syllabus/ Mode of Selection for the Post of Assistant Registrar with reference to the Advt. No: IIITR/RG/2026/Advt./01 Date: 30.01.2026

Group – A

2. **Assistant Registrar:**

In view of the large number of applications received for the post of Assistant Registrar, the Institute has decided to conduct a Screening Test. There shall be three stages of the selection process. Candidates shortlisted in **Stage–I (Screening Test)** shall appear in **Stage–II (Presentation Round)** on the syllabus prescribed for Stage–I. Based on their performance in the Presentation Round, candidates will be further shortlisted for the final round, i.e., **Stage–III (Personal Interview).**

Stage – I: Screening Test: 50 MCQ Type Questions of 01-hour duration with no negative marking:

- General Awareness and Current Affairs
- **Aptitude Test -** Quantative Aptitude, Numerical Ability, Data Interpretation, Logical Reasoning & Computer Aptitude.
- **English -** Grammar & Comprehension.
- Constitution of India.
- General Awareness related to IIIT Ranchi as per the data mentioned on the website.
- IIIT (PPP) Act and Statutes of IIIT Ranchi.
- UG, PG and Ph.D. Ordinances of IIIT Ranchi.
- Policies and Regulatory Bodies of Govt. of India on Higher Technical Education.
- RTE Act, RTI Act 2005, Goods and Services Tax (GST), National Education Policy (NEP) 2020, National Pension Scheme (NPS), General Provident Fund (GPF)
- FR and SR rules covering Service Matter, Pay Fixation, TA/DA rules, LTC Rules, Foreign Services, Deputation, Lien, Advances.
- Allowances including Children Education Allowance (CEA), Medical Attendance Rules (CGHS & CSMA)
- CCS (Pension) Rule, CCS (Conduct) Rule, CCS (CCA) Rule, CCS (Leave) Rule.
- Provision of Central Government Accounts (Receipts and Payments) Rules.
- Income Tax Act 1961 along with Financial Act.
- Recruitment and Reservation Rules.
- Budget and Accounting in Autonomous Bodies.
- General Financial Rules (GFR) 2017 and its subsequent amendments, Policies and rules for Procurement of Goods and Services, CPPP and GeM Portal, Delegation of Financial Rules.
- Rajbhasha Adhiniyam

Stage – II: Presentation Round

During the Presentation Round, the candidates shall be assessed on their domain knowledge relevant to the post, general communication skills, and ability to handle day-to-day administrative matters.

Stage – III: Personal Interview

The Personal Interview shall be conducted by the Selection Committee to examine the suitability of the candidates for the said post, inter alia, on the basis of their academic qualifications, domain expertise, relevant experience, general awareness, communication skills, and overall personality.

The final merit list shall be prepared solely on the basis of the candidate's performance in the Personal Interview (Stage–III). Stage–I (Screening Test) and Stage–II (Presentation Round) shall be conducted only for the purpose of screening/shortlisting the candidates for the subsequent stage.

Syllabus/ Mode of Selection for the Post of Junior Superintendent with reference to the Advt. No: IIITR/RG/2026/Advt./01 Date: 30.01.2026

Group - B

3. **Junior Superintendent:**

There shall be three stages in the selection process, namely **Stage–I (Screening Test), Stage–II (Skill Test), and Stage–III (Domain Test)**. Stage–I is merely for screening/shortlisting of the candidates for the next stage.

Stage – I: Screening Test: 50 MCQ Type Questions of 01-hour duration with no negative marking:

- General Awareness and Current Affairs
- **Aptitude Test -** Quantative Aptitude, Numerical Ability, Data Interpretation, Logical Reasoning & Computer Aptitude.
- **English -** Grammar & Comprehension.
- Constitution of India.
- Basic Knowledge of Government Policies.
- General Awareness related to IIIT Ranchi as per the data mentioned on the website.
- IIIT (PPP) Ranchi Act and Statutes, UG, PG and Ph.D. Ordinances of IIIT Ranchi.
- Policies and Regulatory Bodies of Govt. of India on Higher Technical Education.
- RTE Act, Income Tax Act, RTI Act 2005, Goods and Service Tax (GST), National Education Policy (NEP) 2020, National Pension Scheme (NPS), General Provident Fund (GPF).
- Allowances including Children Education Allowance (CEA), HRA, TA, DA, LTC and other applicable allowances.
- Medical Attendance Rules (CGHS & CSMA)
- CCS (Pension) Rule, CCS (Conduct) Rule, CCS (CCA) Rule, CCS (Leave) Rule.
- General Financial Rules (GFR) 2017 and its subsequent amendments, Policies and rules for Procurement of Goods and Services, CPPP and GeM Portal.
- Recruitment and Reservation Rules.
- Rajbhasha Adhiniyam

Stage – II: Skill Test: 50 marks of 30 minutes duration:

- Typing, M.S. Word, MS- Excel, MS-PowerPoint, Internet, E-Mail, Dictation etc.

Stage – III: Domain Test: 50 marks of 01-hour duration:

Descriptive Test –

- Essay, Comprehension, Paragraph, Letter Writing, Basic Grammar of English and its usage, Noting/Drafting/D.O. Letter/Notification/Circular.

The final merit list shall be prepared based on 40% weightage of the marks obtained in Stage–II (Skill Test) and 60% weightage of the marks obtained in Stage–III (Domain Test).

Syllabus/ Mode of Selection for the Post of Junior Assistant with reference to the Advt. No: IIITR/RG/2026/Advt./01 Date: 30.01.2026

Group - C

4. Junior Assistant:

There shall be three stages in the selection process, namely **Stage–I (Screening Test), Stage–II (Skill Test), and Stage–III (Domain Test)**. Stage–I is merely for screening/shortlisting of the candidates for the next stage.

Stage – I: Screening Test: 50 MCQ Type Questions of 01-hour duration with no negative marking:

- General Awareness and Current Affairs
- **Aptitude Test -** Quantative Aptitude, Numerical Ability, Data Interpretation, Logical Reasoning & Computer Aptitude.
- **English -** Grammar & Comprehension.
- Constitution of India.
- Basic Knowledge of Government Policies.
- General Awareness related to IIIT Ranchi as per the data mentioned on the website.
- IIIT (PPP) Act and Statutes of IIIT Ranchi.
- Policies and Regulatory Bodies of Govt. of India on Higher Technical Education.
- RTE Act, Income Tax Act, RTI Act 2005, Goods and Services Tax (GST), National Education Policy (NEP) 2020.
- CCS (Leave) Rules, GFR 2017 and its subsequent amendments.
- Rules and Policies for procurement of Goods and Services, Tendering Process, CPPP, GeM Portal etc.
- Allowances including Children Education Allowance (CEA), HRA, TA, DA, LTC and other applicable allowances.

Stage – II: Skill Test: 50 marks of 30 minutes duration:

- Typing, M.S. Word, MS- Excel, MS-PowerPoint, Internet, E-Mail, Dictation etc.

Stage – III: Domain Test: 50 marks of 01-hour duration:

Descriptive Test – Essay, Comprehension, Paragraph, Letter Writing, Basic Grammar of English and its usage.

The final merit list shall be prepared based on 40% weightage of the marks obtained in Stage–II (Skill Test) and 60% weightage of the marks obtained in Stage–III (Domain Test).

Syllabus/ Mode of Selection for the Post of Junior Technician (CSE) with reference to the Advt. No: IIITR/RG/2026/Advt./01 Date: 30.01.2026

Group – C

5. **Junior Technician (Lab) – Computer Science and Engineering (CSE):**

There shall be two stages in the selection process, namely **Stage–I (Domain Test) and Stage–II (Skill Test).**

Stage – I: Domain Test: 50 MCQ Type Questions of 01-hour duration with no negative marking:

➢ **Part -A: General Aptitude:**

- General Awareness and Current Affairs
- Aptitude Test: Quantitative Aptitude, Numerical Ability, Data Interpretation, Logical Reasoning and Computer Aptitude
- English: Grammar and Comprehension.
- MS Word, Excel, Power point, Internet, Email.
- Drafting of letters, notices, other forms of communications in English

➢ **Part-B: Technical:**

- **Programming and Data Structures:** Programming in C & C++, Arrays, Linked List, Stacks, Queues, Trees, Graphs, Searching, Sorting, Hashing, Graph Traversals and File Handling.
- **Operating System:** Basic Concepts of Operating System, Process & Process Scheduling, Threads, Inter-Process Communication, Synchronization, Deadlock, CPU and I/O Scheduling, Memory Management, Virtual Memory, File Systems, Linux/Unix Commands, Shell Scripting.
- **Computer Organization:** Combinational and Sequential Circuits, Adder, Subtractor, MUX/DEMUX, Encoder, Decoder, PROM, RAM, Cache, Main Memory, I/O interface, Control Unit, Addressing Mode, Memory Interfacing.
- **Computer Networks:** Basic Concepts of Networking, OSI and TCP/IP Protocol Stack, Basics of Packet, Circuit and Virtual Circuit Switching, IP addressing, IPv4, IPv6, Basics of IP Support Protocols (ARP, DHCP, ICMP), Network Address Translation (NAT), UDP, TCP, DNS, SMTP, HTTP, FTP, Email.
- **Databases:** Basic Concepts of DBMS, ER-Model, Relational Model, Relational Algebra, Transactions and Concurrency Control, SQL Queries.
- **Software Engineering**: Software Development Life Cycle, Requirements Engineering, System Design, Modeling, Coding Practices, Testing.

- **Web Designing:** Fundamental Design Principles, UI/UX, Front-End Technologies (HTML, CSS, JavaScript).

Stage – II: Skill Test: 50 marks of 30 minutes duration:

- Programming test using C/C++/Python: Programming in C & C++, Arrays, Linked List, Stacks, Queues, Trees, Graphs, Searching, Sorting, Hashing, Graph Traversals and File Handing and Object-Oriented Programming Concepts.

The final merit list shall be prepared by assigning 60% weightage to the Domain Test and 40% weightage to the Skill Test, subject to the condition that only those candidates who score 40% or above marks (General/EWS) and 35% marks (SC/ST/OBC-NCL) in Stage–II (Skill Test) shall be considered for preparation of the final merit list.

Syllabus/ Mode of Selection for the Post of Junior Technician (ECE) with reference to the Advt. No: IIITR/RG/2026/Advt./01 Date: 30.01.2026

Group – C

6. **Junior Technician (Lab) – Electronics and Communication Engineering (ECE):**

There shall be two stages in the selection process, namely **Stage–I (Domain Test) and Stage–II (Skill Test).**

Stage – I: Domain Test: 50 MCQ Type Questions of 01-hour duration with no negative marking:

➤ **Part -A: General Aptitude:**

- General Awareness and Current Affairs
- Aptitude Test: Quantitative Aptitude, Numerical Ability, Data Interpretation, Logical Reasoning and Computer Aptitude
- English: Grammar and Comprehension.
- MS Word, Excel, Power point, Internet, Email.
- Drafting of letters, notices, other forms of communications in English

➤ **Part-B: Technical:**

- **Electronic Devices & Circuits:** Energy Bands in Intrinsic and Extrinsic Semiconductors, Equilibrium Carrier Concentration, Direct and Indirect Band-Gap Semiconductors, Carrier Transport: Diffusion Current, Drift Current, Mobility and Resistivity, Generation and Recombination of Carriers, Poisson and Continuity Equations. P-N Junction, Zener diode, BJT, MOS Capacitor, MOSFET, LED, Photo Diode and Solar Cell.
- **Digital Logic & Design**: Number Representations: Binary, Integer and Floating-point-Numbers. Combinatorial Circuits: Boolean Algebra, Minimization of functions using Boolean Identities and Karnaugh Map, Logic Gates and their static CMOS Implementations, Arithmetic Circuits, Code Converters, Multiplexers, Decoders. Sequential Circuits: Latches and Flip-Flops, Counters, Shift-Registers, Finite State Machines, Propagation Delay, Setup and Hold Time, Critical Path Delay. Data Converters: Sample and Hold Circuits, ADCs and DACs, Semiconductor Memories: ROM, SRAM, DRAM.
- **Analog & Linear Integrated Circuit:** Diode Circuits: Clipping, Clamping and Rectifiers. Amplifiers: Biasing, AC Coupling, Small Signal Analysis, Frequency Response. Current Mirrors and Differential Amplifiers. Op-amp Circuits: Amplifiers, Summers, Differentiators, Integrators, Active Filters, and Oscillators.

- **Circuit Analysis & Synthesis:** Node and Mesh Analysis, Superposition, Thevenin's Theorem, Norton's Theorem, Reciprocity. Sinusoidal Steady State Analysis: Phasors, Complex Power, Maximum Power Transfer. Time and Frequency Domain Analysis of Linear Circuits: RL, RC and RLC Circuits, Solution of Network Equations using Laplace Transform.

- **Microprocessors and Microcontrollers:** Microprocessor and Micro Computer, 8085 Microprocessor Architecture, 8085 Microprocessor Pin Diagram and its functionality, Register Organization, System Bus Structure, and Interrupts, Addressing Modes of 8085, Instruction Set of 8085, Instruction Types of 8085, Assembly Language Programming of 8085, Memory and I/O Interfacing, Processor Execution Process of Machine Instruction (Instruction Timing Diagram Analysis)

- **Signals and Systems:** Continuous-time Signals: Fourier series and Fourier Transform, Sampling Theorem and Applications, Discrete-Time Signals: DTFT, DFT, z-transform, Discrete-time Processing of Continuous-Time Signals. LTI systems: Definition and Properties, Causality, Stability, Impulse Response, Convolution, Poles and Zeroes, Frequency Response, Group Delay, Phase Delay.

- **Analog Communication:** Random Processes: Auto Correlation and Power Spectral Density, Properties of White Noise, Filtering of Random Signals through LTI Systems. Analog Communications: Amplitude Modulation and Demodulation, Angle Modulation and Demodulation, Spectra of AM and FM, Super Heterodyne Receivers. Information Theory: Entropy, Mutual Information and Channel Capacity Theorem.

- **Digital Communication:** PCM, DPCM, Digital Modulation Schemes (ASK, PSK, FSK, QAM), Bandwidth, Inter-Symbol Interference, MAP, ML Detection, Matched Filter Receiver, SNR and BER. Fundamentals of Error Correction, Hamming Codes, CRC.

Stage-II: Skill Test (50 Marks, 30 Minutes Duration)

- Device Identification, Lab Management, Laboratory Experiments related to the subjects of Basic Electronics, Digital Electronics, Microprocessor and Microcontroller

➤ **Lab Syllabus:**

Basic Electronics (or Electronic Devices and Circuits):

- **Diodes:** Semiconductor Diode, V-I characteristics of Diode, Half-Wave and Full-Wave Rectifier Circuits, Wave Shaping Circuits, Clippers and Clampers, Zener Diodes. **Transistors:** Bipolar Junction Transistor, **MOSFET:** Biasing, Small Signal model, Amplifiers. **Operational Amplifiers:** Ideal Op-Amp, **Application of Op-Amp:** Comparator, Inverting and non-Inverting Amplifiers, Differential and Integral Amplifier, Adder-Subtractor.

- **Digital Electronics:** Logic Gates and Combinational Circuits: Combinational Logic Circuits, Binary Half and Full adder-subtractor, Parity Generator-Checker, Sequential Circuits, Storage Elements; NAND and NOR gate Latches, S-R Flip-Flop, J-K Flip-Flop, D Flip-Flop, T- Flip- Flop, , MUX/DEMUX, Counters, Sample and hold circuits, ADCs and DACs, Semiconductor Memories: ROM, SRAM, DRAM.

- **Microprocessor and Microcontroller:** Microprocessor and Micro Computer, 8085 Microprocessor Architecture, 8085 Microprocessor Pin Diagram and its functionality, Register Organization, System Bus Structure, and Interrupts, Addressing Modes of 8085, Instruction Set of 8085, Instruction Types of 8085, Assembly Language Programming of 8085, Memory and I/O Interfacing, Processor Execution Process of Machine Instruction (Instruction Timing Diagram Analysis)

The final merit list shall be prepared by assigning 60% weightage to the Domain Test and 40% weightage to the Skill Test, subject to the condition that only those candidates who score 40% or above marks (General/EWS) and 35% marks (SC/ST/OBC-NCL) in Stage–II (Skill Test) shall be considered for preparation of the final merit list.

Syllabus/ Mode of Selection for the Post of Junior Technician (Library) with reference to the Advt. No: IIITR/RG/2026/Advt./01 Date: 30.01.2026

Group – C

7. **Junior Technician (Library):**

There shall be two stages in the selection process, namely **Stage–I (Domain Test) and Stage–II (Skill Test).**

Stage – I: Domain Test: 50 MCQ Type Questions of 01-hour duration with no negative marking:

➢ **Part -A: General Aptitude:**

- General Awareness and Current Affairs
- Aptitude Test: Quantitative Aptitude, Numerical Ability, Data Interpretation, Logical Reasoning and Computer Aptitude
- English: Grammar and Comprehension.
- MS Word, Excel, Power point, Internet, Email.
- Drafting of letters, notices, other forms of communications in English

➢ **Part-B: Domain Knowledge:**

- **Library and Society:** Laws of Library Science; Types of Libraries; Library Associations, Systems and Programmes; History, Library Movement and Library Legislation in India; Organizations and Institutions involved in the development of Library and Information Services - UNESCO, IFLA, FID, INIS, etc.
- **Library Management:** Collection development and Selection Principles, Acquisition Procedure for books, journals, Library Personnel and Library Committee, Library Rules and Regulations; Library Finance and Budget; Human Resource Management; Principles of Library Management, Library organization and Structure; Use and Maintenance of the Library - Circulation, Maintenance, Shelving, Stock Verification, Binding and Preservation, Weeding out, etc.
- **Knowledge Organization: Library Classification and Cataloguing:** Canons and Principles, Library Classification Schemes - DDC, CC, UDC; Library Cataloguing Codes-CCC and AACR; ISBD; MARC; CCF; ISBN; ISSN; etc.
- **Reference and Information Sources and services:** Types of information resources, Bibliography and Reference Sources; Sources of Information - Primary, Secondary, Tertiary; digital documents; Information Services: e-resources, Consortia, eShodhsindhu, etc. Concept and need for Information; Types of Documents; Nature and organization of Information Services, Abstracting and Indexing Services; Computer based Information Services - CAS, SDI; Information retrieval, etc., One Nation One Subscription (ONOS).

- **Information Storage and Retrieval:** Information Storage and Retrieval Systems - Sears List, PRECIS, POPSI, KWIC etc.; Vocabulary Control; Search Strategies; Evaluation of Information Retrieval Systems etc.
- **Information Technology, Recent ICT trends in Libraries:** Generations of Computer; Classification of Computers; Computer memory and their types; Computer Architecture; I/O devices; Programming Languages & Operating Systems; Application Software; Library Automation and software packages; Internet; Digital Libraries; RFID; Networks - DELNET, NICNET, etc.; National and International Information Systems-NASSDOC, NISCAIR, DESIDOC; etc.

Stage-II: Skill Test (50 Marks, 30 Minutes Duration)

- Based on the domain syllabus of Stage-I and Knowledge of Library Automation, Relevant Software and day-to-day Library Operations.

The final merit list shall be prepared by assigning 60% weightage to the Domain Test and 40% weightage to the Skill Test, subject to the condition that only those candidates who score 40% or above marks (General/EWS) and 35% marks (SC/ST/OBC-NCL) in Stage–II (Skill Test) shall be considered for preparation of the final merit list.